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EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,769	ABRAMSON ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 30 have been examined.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 1 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 1 recites, "reclaiming resources" in line 7. Reclaiming resources, as recited in claim 1, provides no tangible result. Examiner suggests revising claim 1 to recite that the reclaiming resources comprises updating a memory, freeing a memory, etc., so as to provide a tangible result. Please refer to pages 48 – 49 of the Interim Guidelines published October 26, 2005.

Claims 11, 21 and 27 are rejected under similar rationale.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (f) he did not himself invent the subject matter sought to be patented.

Claims 1 – 10, and 21 – 30 are rejected under 35 U.S.C. 102(a) as being anticipated by Howard et al. (Enhanced Host Controller Interface Specification for Universal Serial Bus – Revision 0.95).

Regarding claim 1, Howard et al. describe a method comprising:

Removing a work item of a plurality of work items from an enabled expansion bus schedule data structure (page 68, section 4.8.2);

Generating a coherency signal (interpreted as an Interrupt on Async Advance Doorbell bit) independent of said work item utilizing an expansion bus host controller in response to removing said work item from said enabled expansion bus schedule data structure (page 69);

Reclaiming resources assigned to said work item whenever said coherency signal is generated (page 69).

Regarding claim 2, Howard et al. describe wherein said enabled expansion bus schedule data structure comprises an asynchronous schedule including a plurality of queue heads and removing said work item from said enabled expansion bus schedule data structure comprises unlinking a first queue head of said plurality of queue heads from said asynchronous schedule (pages 68 – 69, section 4.8.2).

Regarding claim 3, Howard et al. describe wherein said plurality of queue heads includes a second queue head, said second queue head includes a horizontal link pointer to said first queue head, and unlinking said first queue head from said

asynchronous schedule comprises modifying said horizontal link pointer of said second queue head (pages 68 – 69, section 4.8.2).

Regarding claim 4, Howard et al. describe the method further comprising:

Generating a command signal in response to removing said work item from said enabled expansion bus data structure (page 69); wherein,

Generating a coherency signal utilizing an expansion bus host controller in response to removing said work item from said enabled expansion bus schedule data structure comprises generating a status signal utilizing said expansion bus host controller in response to generating said command signal (page 69).

Regarding claim 5, Howard et al. describe wherein generating a coherency signal utilizing an expansion bus host controller in response to removing said work item from said enabled expansion bus schedule data structure comprises:

Traversing said plurality of work items according to a sequence;

Storing a copy of a work item within a memory in response to traversing said plurality of work items;

Generating a coherency signal utilizing said copy of said work item (pages 68 – 69, section 4.8.2).

Regarding claim 6, Howard et al. teach wherein generating a coherency signal utilizing said copy of said work item comprises:

Detecting a removal of said copy of said work item from said memory in response to removing said work item from said enabled expansion bus schedule data structure; and

Generating a coherency signal (interpreted as an Interrupt on Async Advance bit) in response to detecting said removal of said copy of said work item from said memory (page 69).

Regarding claim 7, Howard et al. describe wherein detecting a removal of said copy of said work item from said memory in response to removing said work item from said enabled expansion bus schedule data structure comprises detecting a cache flush operation (interpreted as the host controller releasing all on-chip state; page 69).

Regarding claim 8, Howard et al. describe wherein generating a coherency signal utilizing said copy of said work item comprises:

Identifying an accessible work item of said plurality of work items utilizing said copy of said work item;

Generating a coherency signal (interpreted as setting a status bit) in response to traversing beyond said accessible work item in said sequence (page 69).

Regarding claim 9, Howard et al. describe the method further comprising:

Executing a transaction on a Universal Serial Bus in response to traversing said plurality of work items (interpreted as setting a status bit; page 69).

Regarding claim 10, Howard et al. describe the method further comprising storing each of said plurality of work items within a memory, wherein reclaiming said work item in response to generating said coherency signal comprises freeing a portion of said memory associated with said work item (page 69 indicates that data structures (such as queue heads) are associated with memory, and that this memory can be freed following a handshake mechanism (interpreted as a coherency signal)).

Regarding claim 21, Howard et al. describe an apparatus comprising:

A command register (interpreted as a USBCMD register) including a command signal bit (interpreted as an Interrupt on Async Advance Doorbell bit) to indicate a removal of a work item from an expansion bus schedule data structure including a plurality of work items, wherein the command signal bit is independent of the work item (page 69);

A status register (interpreted as a USBSTS register) including a status signal bit (interpreted as an Interrupt on Async Advance bit) to notify an expansion bus host controller driver that resources assigned to said work item may be reclaimed (page 69); and

A microcontroller (interpreted as a host controller; page 3) to process said expansion bus schedule data structure and to modify said status signal bit of said status register in response to said removal of said work item from said expansion bus schedule data structure (page 69).

Regarding claim 22, Howard et al. describe wherein said expansion bus schedule data structure comprises a Universal Serial Bus (USB) asynchronous schedule (page 67).

Regarding claim 23, Howard et al. describe the apparatus further comprising a cache memory to store a copy of a work item (page 68 alludes to the fact that the host controller retains a cached copy of a work item); wherein said microcontroller to process said expansion bus schedule data structure and to modify said status signal bit of said status register comprises:

A microcontroller to traverse said plurality of work items according to a sequence, to store said copy of said work item within said cache memory, and to modify said status signal bit (interpreted as an Interrupt on Async Advance bit) of said status register (interpreted as a USBSTS register) utilizing said copy of said work item (page 69).

Regarding claim 24, Howard et al. describe wherein said microcontroller to modify said status signal bit of said status register utilizing said copy of said work item comprises:

A microcontroller to modify said status signal bit (interpreted as an Interrupt on Async Advance bit) of said status register (interpreted as a USBSTS register) in

response to a removal of said copy of said work item from said cache memory (page 69).

Regarding claim 25, Howard et al. describe wherein said microcontroller to modify said status signal bit of said status register in response to a removal of said copy of said work item from said cache memory comprises a microcontroller to modify said status signal bit of said status register in response to a cache flush operation (interpreted as the host controller releasing all on-chip state; page 69).

Regarding claim 26, Howard et al. describe wherein said microcontroller to modify said status signal bit of said status register utilizing said copy of said work item comprises:

A microcontroller to identify an accessible work item of said plurality of work items utilizing said copy of said work item and to modify said status signal bit of said status register in response to a traversal beyond said accessible work item in said sequence (page 69).

Regarding claim 27, Howard et al. describe a computer system comprising:

A memory to store an expansion bus schedule data structure including a plurality of work items (page 4, Figure 1-3);

An expansion bus host controller (interpreted as a Host Controller; page 3) comprising:

A command register (interpreted as a USBCMD register) including a command signal bit (interpreted as a Interrupt on Async Advance Doorbell bit) independent of the plurality of work items (page 69);

A status register (interpreted as a USBSTS register) including a status signal bit (interpreted as an Interrupt on Async Advance bit; page 69);

A microcontroller to process said expansion bus schedule data structure and to modify said status signal bit of said status register inr esponse toa modification of said command signal bit (page 69);

A processor to remove a work item of said plurality of work items from said expansion bus schedule data structure, to modify said command signal bit in response to said removal of said work item from said expansion bus schedule data structure; and

To reclaim resources assigned to said work item in response to a modification of said status signal bit (pages 68 – 69, section 4.8.2).

Regarding claim 28, Howard et al. describe the apparatus further comprising a cache memory to store a copy of a work item (page 68 alludes to the fact that the host controller retains a cached copy of a work item); wherein said microcontroller to process said expansion bus schedule data structure and to modify said status signal bit of said status register comprises:

A microcontroller to traverse said plurality of work items according to a sequence, to store said copy of said work item within said cache memory, and to modify said status signal bit (interpreted as an Interrupt on Async Advance bit) of said status

register (interpreted as a USBSTS register) utilizing said copy of said work item (page 69).

Regarding claim 29, Howard et al. describe wherein said microcontroller to modify said status signal bit of said status register utilizing said copy of said work item comprises:

A microcontroller to modify said status signal bit (interpreted as an Interrupt on Async Advance bit) of said status register (interpreted as a USBSTS register) in response to a removal of said copy of said work item from said cache memory (page 69).

Regarding claim 30, Howard et al. describe wherein said microcontroller to modify said status signal bit of said status register utilizing said copy of said work item comprises:

A microcontroller to identify an accessible work item of said plurality of work items utilizing said copy of said work item and to modify said status signal bit of said status register in response to a traversal beyond said accessible work item in said sequence (page 69).

* * *

Claims 1 – 30 are rejected under 35 U.S.C. 102(f) because the applicant did not invent the claimed subject matter. "Significant Contributors" of the Enhanced Host Controller Interface Specification for Universal Serial Bus (third page from cover) recites individuals that are not named as inventors in the instant application.

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> 210 forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

215 The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
220 3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 11 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over

225 Howard et al. in view of Ritchie (U.S. 4,135,240).

Regarding claim 11, Howard et al. teach a method comprising:

Removing a work item of a plurality of work items from an enabled expansion bus schedule data structure (page 68, section 4.8.2);

Generating a coherency signal (interpreted as an Interrupt on Async Advance Doorbell bit) independent of said work item utilizing an expansion bus host controller in response to removing said work item from said enabled expansion bus schedule data structure (page 69);

Reclaiming resources assigned to said work item whenever said coherency signal is generated (page 69).

Howard et al. fail to explicitly teach a computer program product in a recordable-type media that provides instructions which when executed bya machine cause said machine to perform the operations.

Ritchie teaches that computer hardware and software are functionally equivalent and interchangeable, as well as that one may be preferable to another depending on the situation (column 5, lines 48 – 60).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement the method of Howard et al. into a computer program product for the purpose of debugging, simulation, or simpler design modification.

Regarding claim 12, Howard et al. teach the additional limitation wherein said enabled expansion bus schedule data structure comprises an asynchronous schedule including a plurality of queue heads and removing said work item from said enabled expansion bus schedule data structure comprises unlinking a first queue head of said plurality of queue heads from said asynchronous schedule (pages 68 – 69, section 4.8.2).

Regarding claim 13, Howard et al. teach the additional limitation wherein said plurality of queue heads includes a second queue head, said second queue head includes a horizontal link pointer to said first queue head, and unlinking said first queue head from said asynchronous schedule comprises modifying said horizontal link pointer of said second queue head (pages 68 – 69, section 4.8.2).

Regarding claim 14, Howard et al. teach the additional limitation the method further comprising:

Generating a command signal in response to removing said work item from said enabled expansion bus data structure (page 69); wherein,

Generating a coherency signal utilizing an expansion bus host controller in response to removing said work item from said enabled expansion bus schedule data structure comprises generating a status signal utilizing said expansion bus host controller in response to generating said command signal (page 69).

Regarding claim 15, Howard et al. teach the additional limitation wherein generating a coherency signal utilizing an expansion bus host controller in response to removing said work item from said enabled expansion bus schedule data structure comprises:

Traversing said plurality of work items according to a sequence;

Storing a copy of a work item within a memory in response to traversing said plurality of work items;

Generating a coherency signal utilizing said copy of said work item (pages 68 – 69, section 4.8.2).

Regarding claim 16, Howard et al. teach wherein generating a coherency signal utilizing said copy of said work item comprises:

Detecting a removal of said copy of said work item from said memory in response to removing said work item from said enabled expansion bus schedule data structure; and

Generating a coherency signal (interpreted as an Interrupt on Async Advance bit) in response to detecting said removal of said copy of said work item from said memory (page 69).

Regarding claim 17, Howard et al. teach the additional limitation wherein detecting a removal of said copy of said work item from said memory in response to removing said work item from said enabled expansion bus schedule data structure comprises detecting a cache flush operation (interpreted as the host controller releasing all on-chip state; page 69).

Regarding claim 18, Howard et al. teach the additional limitation wherein generating a coherency signal utilizing said copy of said work item comprises:

Identifying an accessible work item of said plurality of work items utilizing said copy of said work item;

Generating a coherency signal (interpreted as setting a status bit) in response to traversing beyond said accessible work item in said sequence (page 69).

Regarding claim 19, Howard et al. teach the additional limitation the method further comprising:

Executing a transaction on a Universal Serial Bus in response to traversing said plurality of work items (interpreted as setting a status bit; page 69).

Regarding claim 20, Howard et al. teach the additional limitation the method further comprising storing each of said plurality of work items within a memory, wherein reclaiming said work item in response to generating said coherency signal comprises freeing a portion of said memory associated with said work item (page 69 indicates that data structures (such as queue heads) are associated with memory, and that this memory can be freed following a handshake mechanism (interpreted as a coherency signal)).

Response to Arguments

Applicant's arguments, filed 6/12/2006, with respect to the rejection(s) of claim(s) 1 - 20 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new

ground(s) of rejection is made in view of Howard et al. (Enhanced Host Controller Interface Specification for Universal Serial Bus – Revision 0.95).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MDS

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